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IPSILIUM LLC

IN THE UNITED STATES DISTRICT COURT

FOR THE NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

IPSILIUM LLC, Plaintiff, v. CISCO SYSTEMS, INC., Defendant.	Case No. COMPLAINT FOR PATENT INFRINGEMENT DEMAND FOR JURY TRIAL

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Ipsilium LLC ("Ipsilium"), as its Complaint for Patent Infringement against Cisco Systems, Inc. ("Defendant" or "Cisco"), alleges as follows:

THE PARTIES

1. Ipsilium is a Limited Liability Company established and existing under the laws of the State of California, with a mailing address at 947 Edinburgh Street, San Francisco, California. Ipsilium is the owner by assignment of all right, title and interest in U.S. Patents 6, 819,681 B1 ("the '681 patent") and 6,961,777 B1 ("the '777 patent) (collectively the "Ipsilium patents" or "patents-in-suit"). A copy of the '681 patent is attached hereto as Exhibit 1. A copy of the '777 patent is attached hereto as Exhibit 2.

2. On information and belief, Cisco is a corporation established and existing under the laws of the State of California with its principal place of business at 170 West Tasman Drive, San Jose, California 95134. Cisco may be served through its agent for service of process CSC at 2710 Gateway Oaks Dr. Ste. 150N, Sacramento, CA 95833.

JURISDICTION AND VENUE

3. This is an action for patent infringement arising under the patent laws of the United States, 35 U.S.C. §1, *et seq.* This Court has subject matter jurisdiction under 28 U.S.C. §1338.

4. This Court has personal jurisdiction over defendant Cisco at least because Cisco resides in this judicial district, has its principal place of business and several other established places of business in this district, routinely conducts business in this district and has committed acts that constitute infringement of the patents-in-suit in this district.

5. Venue is proper in this district pursuant to 28 U.S.C. §1400(b).

INTRADISTRICT ASSIGNMENT

6. This is an Intellectual Property action appropriate for district-wide assignment under Civ. L. R. 3-2(c).

IPSILIUM'S INNOVATIONS

7. Ipsilium incorporates herein by reference each and every allegation set forth in paragraphs 1 - 6 above.

8. Shrikumar Hariharasubrahmanian is the sole inventor of the '681 and '777 patents and an owner of Ipsilium.

9. Dr. Hariharasubrahmanian earned a Bachelor of Engineering degree, with honors, in Electrical and Electronics Engineering from Birla Institute of Technology and Science (BITS) in Pilani, India in 1987. Upon graduating from BITS, he joined Hindustan Computers Ltd. (HCL) in Noida, India, where his responsibilities included developing networking hardware and memory boards for multiprocessor and clustered Unix machines. He then joined the National Centre for Software Technology (NCST) in Mumbai, India, where he was involved in designing and deploying the first Internet-connected network in India. The Education and Research Network (ERNET) established TCP/IP connectivity between universities and research institutions and connected those institutions to others throughout the world. He later served as President at Temporal Systems in Bombay, India, which was a solution provider that consulted to the first company licensed to provide value-added Internet services in India. Dr. Hariharasubrahmanian contributed to architecting the company's network, designing its email service and planning its business strategy.

10. In 1993 Dr. Hariharasubrahmanian enrolled as a graduate student in the Electrical and Computer Engineering program at the University of Massachusetts, Amherst, where he was awarded a Ph.D. in Computer Science in 2003. While earning his Ph.D., Dr. Hariharasubrahmanian also worked as a research scientist at the Massachusetts Institute of Technology Media Lab.

11. In 1998 Dr. Hariharasubrahmanian learned of an announcement regarding the smallest TCP/IP web server computer yet made. That computer, which was reportedly about the size of a matchbox, consisted of an x486 microprocessor, 16 megabytes ("MB") of random access memory ("RAM"), and 16 MB of flash read-only memory ("ROM"). Dr. Hariharasubrahmanian believed that such a server could be made to run on a considerably smaller system, and he set about tackling that design challenge.

12. In fact, Dr. Hariharasubrahmanian decided he would greatly increase the level of difficulty of the design challenge by starting with the smallest commercially available microcontroller chip then available, the PIC 12C508 microcontroller from Microchip Technology Inc. That chip, normally used to control the limited functions of home appliances, included just 512 bytes of ROM, 25 bytes of RAM and one peripheral input/output ("I/O") port. Dr. Hariharasubrahmanian succeeded in programing that device as a reliable, fully TCP/IP compliant web server, using only 5 bytes of RAM.

13. Dr. Hariharasubrahmanian's accomplishment was lauded worldwide. For example, in an article titled "Tiniest Web Server," Popular Science Magazine described his computer as the "smallest computer ever built" that also "understands TCP/IP." *See* Murray Slovick, Jan. 2000, at 38, *available at* https://books.google.com/books?id=GppZTYajC_AC&pg=PA38. Science Daily described it as "the world's smallest" computer that is the size of a "match-head" while being "fully compliant with the requirements of the [TCP/IP] standards." *See* "UMass Computer Science Graduate Student Builds World's Tiniest Web-Server", Aug. 11, 1999, *available at* https://www.sciencedaily.com/releases/1999/08/990811075627.htm. Other publications reporting the achievement included: Wired Magazine (Leander Kahney, "The World's Smallest Server", Aug. 14, 1999, *available at* https://www.wired.com/1999/08/the-worlds-smallest-server/); Associated Press ("Researcher builds inexpensive, aspirin-size Internet computer", Aug. 15, 1999, *available at* http://chronicle.augusta.com/stories/1999/08/15/tec_267945.shtml); The New York Times (Jennifer Lee, "As Small as a Match Tip, This Server Costs 49 Cents", Aug. 19, 1999, *available at* http://www.nytimes.com/1999/08/19/technology/news-watch-as-small-as-a-match-tip-this-server-costs-49-cents.html); ABC News ("Fingernail-sized web server could spread net wider", Aug. 11, 1999, *available at* http://www.abc.net.au/science/news/stories/1999/43230.htm); The Times Higher Education ("Mini web server wires up intelligent buildings", Sept. 17, 1999, *available at* https://www.timeshighereducation.com/news/mini-web-server-wires-up-intelligent-buildings/148015.article); and Canadian Broadcast News ("Student builds Aspirin-size

Internet computer", Nov. 10, 2000, *available at* http://www.cbc.ca/news/technology/student-builds-aspirin-size-internet-computer-1.183286).

14. Dr. Hariharasubrahmanian was able to vastly reduce the amount of working memory required to perform TCP/IP packet processing because he envisioned a novel and superior way to handle that processing. At the time, the standard method for keeping track of a TCP/IP connection and processing packets received the entire incoming packet into memory and then processed it. That was impossible to implement given the limitations of the iPic's memory. Dr. Hariharasubrahmanian overcame this limitation by developing a technique for accurately and reliably predicting the values of packet fields before they were received, while the packet was incoming, and using the predicted value(s) to perform the necessary processing. This new and radically different technique allowed the iPic to determine the processing result for a packet, including the generation of a responsive packet, before it had even received the full incoming packet.

15. Dr. Hariharasubrahmanian's groundbreaking innovation not only made hardware resource limitations all but irrelevant in packet-switched network devices, it provided another highly-desirable benefit to the performance of such devices – it was extremely fast. Eliminating the typical waiting or "latency" period while the device received and processed each packet enabled such speed. Recognizing the significance of his breakthrough, Dr. Hariharasubrahmanian prepared a provisional patent application and filed it with the U.S. Patent and Trademark Office ("USPTO") on August 6, 1999, before disclosing the iPic to the public. The utility applications that lead to the '681 patent and '777 patent were filed on August 4 and August 7, 2000 respectively, and are entitled to priority based on the provisional application. The '681 patent issued on November 16, 2004 and the '777 patent issued on November 1, 2005.

16. Dr. Hariharasubrahmanian co-founded Ipsil, Inc. to further develop and commercialize products based on his concepts. Ipsil received significant investment funding and entered into development agreements with several leading technology companies. Using Dr. Hariharasubrahmanian's inventions, Ipsil was able to demonstrate reliable and efficient network processors running at 10 Gigabit per second ethernet speeds – a five-fold improvement over the 2

Giabit per second speed considered "fast" at the time. Despite demonstrating its superior technology in both the commercial and government sectors, Ipsil was unable to survive the technology recession and ceased operations in 2006. Dr. Hariharasubrahmanian accepted an invitation to join Oracle Corporation and later moved to Oracle Labs, which was formerly the research group at Sun Microsystems, where he has continued to find innovative ways to improve the speed and efficiency of data processing systems.

17. Ipsilium was formed in 2017 with Dr. Hariharasubrahmanian who assigned it his patents.

OVERVIEW OF NETWORKING TECHNOLOGY

18. Ipsilium incorporates herein by reference each and every allegation set forth in paragraphs 1 - 17 above

19. The significance of the patented inventions is best understood in the context of packet-switched network operation. Such networks range from small home or business Wi-Fi networks, to local and wide area networks established by businesses, government and educational institutions. The disparate equipment used in each such network can establish reliable data communication by implementing standard protocols to send and/or receive data. Data is communicated over such networks in one or more "packets," which are transmitted from a source to a destination by passing through one or more intermediate networking devices.

20. A packet includes some or all of 1) the data making up the actual data to be transferred (i.e. the "payload"), for example the contents of a photograph or the details of a stock transaction, and 2) routing control and other information required for successful transmission. That additional control information may precede the payload ("header") or follow the payload ("trailer"). In this way, packets include information analogous to postal mail: headers are like the envelope with the destination and return address, and the payload consists of the contents to be delivered. Packet headers generally consist of source and destination network addresses, sequencing information, error detection information, and other control information necessary for the packet to be properly routed through the shared network and, if the payload was split amongst multiple packets,

information necessary to properly recombine the payloads. A packet, comprising a payload, headers, and trailers, is formed through a modular process called "encapsulation" that involves a series of steps associated with different "layers" of the data communication process, as shown in Fig. 3 of the '777 Patent:

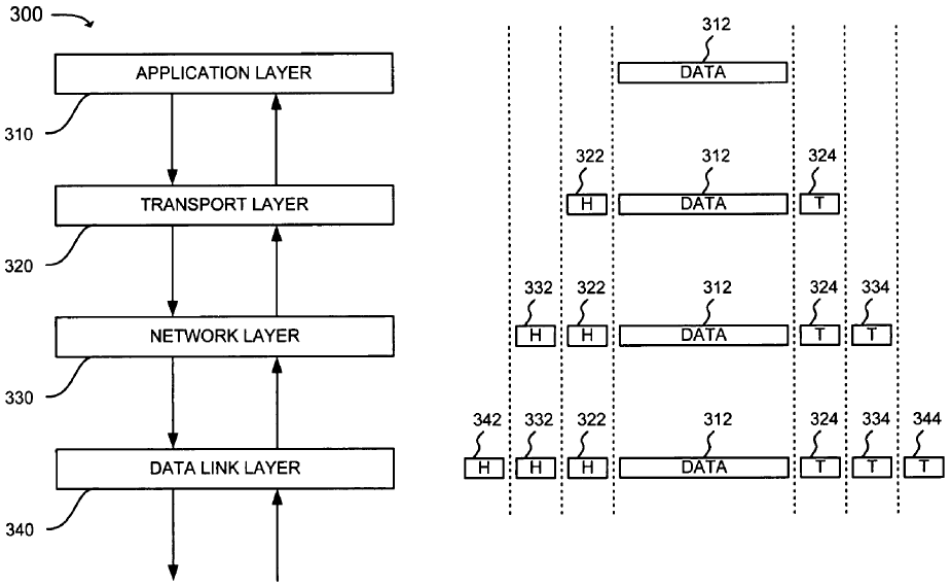


FIG. 3

21. As shown in the Figure above, a packet is generated within a device whereby the data to be transmitted is "encapsulated" with headers, labeled as "H", and trailers, labeled as "T" as each layer acts on the packet. This process of appending additional headers and/or trailers is performed for each successive layer until all the information necessary for successful network transmission has been added to the packet. The header and trailer added for each respective layer are associated with a "protocol" providing rules pertaining to one aspect of communications among networked devices.

22. The information contained in the headers and trailers are necessary for the successful transmission of the packet. For example, the Data Link Layer (also referred to as the Ethernet Layer, Layer 2, or L2) includes device-specific unique identifiers (such as the MAC address) for the sender and for the next device that is to receive the packet. Next, the Network Layer (also referred to as the Internet Layer, Layer 3, or L3) contains the IP addresses for the sender's host device that is

connected to the Internet and the IP address for the receiver's host device. It also contains a time to live ("TTL") field that that indicates the number of intermediate devices the packet may travel through before it is discarded for taking a path that is too long. Finally, for this example, the Transport Layer (also referred to as Layer 4 or L4) contains information that is responsible for establishing a "virtual circuit" between the source and destination devices and may also include a sequence number used to identify where in the stream the packet's payload belongs.

23. The packet is passed from device to device until it reaches the intended final recipient. Each device that receives the packet, including the intended final recipient device, must process the packet according to set protocol standards. The device determines which protocol(s) are present within the packet based on the header (and/or trailer) fields and then analyzes the packet according to the specific protocol. For example, at the Data Link Layer (L2), the current device analyzes the destination address (i.e. the unique identifier) and determines if the address matches the unique identifier of the current device. As another example, at the Network Layer (L3) the device may analyze the TTL field and determine if the packet is still valid. This analysis determines, for example, whether the device should drop the packet.

24. Further, the intermediate or final device may generate a packet in response to the incoming packet. The current device generates that packet according to the relevant protocol. As one example, at the Data Link (L2) Layer, the source address is set to the unique identifier of the current device while the destination address is set to the unique identifier of the device to which the packet is travelling. As another example, the Network (L3) Layer the TTL field may be decremented by one. The current device then transmits a packet that includes the new header fields.

THE PATENTS-IN-SUIT

25. Ipsilium incorporates herein by reference each and every allegation set forth in paragraphs 1 - 24 above.

26. At the time of Dr. Hariharasubrahmanian's invention, networked devices received and stored an incoming packet in memory until sufficient information had been stored for definitive handling according to the relevant protocol's established rules. Only then was a reply packet

generated, and then that packet was transmitted to the appropriate destination. Dr. Hariharasubrahmanian recognized that this serial method added significant and unnecessary delays in packet processing, explaining that "[t]his technique results in increased delays due to the time consumed in storing and processing the packet in two distinct steps." '777 patent at 1:38-39. Such latency in processing caused "inefficiencies or, in some cases, unacceptable performance." *Id.* at 1:63-67; *see also* '681 patent at 2:30-33.

27. Dr. Hariharasubrahmanian's solution to this problem was to begin the processing of header fields before the header fields were received. To enable the processing of header field values not yet known, the patents-in-suit teach that those header field values may be accurately predicted based on other packet fields already received. That is, "the [network] device makes a determination of the ***expected value*** of the value of a packet field later to arrive prior to the actual arrival of the relevant field …" Provisional Application at 4 (emphasis added). That prediction may be made in a variety of ways. For example, the '681 patent explains that certain layers of a communications protocol (e.g. the TCP/IP protocol) "may be arranged to have certain properties constraining their design and selection in a manner that makes the advance determination of packet fields with adequate certainty feasible." '681 patent at 7:54-58. By leveraging the correlation between fields, a received L3 header field, for example, can be used to predict a not-yet-received header field, such as a subsequent field from the same L3 layer or an upper-level L4 header field. In one such case, if the IP packet length header field of the Network Layer (L3) indicates a packet length less than or equal to 39, the protocol field of that Network Layer (L3) is predicted to have a value that identifies the Internet Control Method Protocol ("ICMP"). If the L3 packet length header field is greater than 39, the L3 protocol field is predicted to have a value that identifies the Transmission Control Protocol ("TCP") or User Datagram Protocol ("UDP"). In another case, if the L3 packet length header field is greater than 39 but less than or equal to 58, the synchronization, acknowledge, and finish values of the TCP flags field in the Transport Layer (L4) header can be predicted to be 1, 0, and 0, respectively. If the L3 packet length header field is equal to or greater than 59, on the other hand, the synchronization flag in the TCP flags L4 header field can be predicted as 0. As yet another

example, in the case of fragmented packets the fragment offset field or the sequence number field created by the Transport Layer (L4) can be used to predict the value of the field indicating the portion of the original packet in the current fragment or the length of that fragment data. *See, e.g.,* '681 patent at 8:64-9:8. Accordingly, the Ipsilium patents teach that one or more fields in the packet can be used to predict expected values for one or more other packet fields, without the delay of waiting for the packet fields to be received, stored and read.

28. Thus, rather than following the conventional teaching, which required the network device to sequentially wait to receive each header field before processing according to the relevant protocol, Dr. Hariharasubrahmanian's premised his breakthrough approach on non-linear processing. By recognizing the relationships between fields, his invention permits the accurate ***prediction*** of expected values for subsequent fields and processing based on those expected values, before eventually receiving the actual values. In this way, the Ipsilium patents greatly reduce latency by enabling the processing of future header fields, without having to first wait for them to be received. Thus, the inventions allow for the processing of the packets to be already underway, if not largely completed, before the entire packet is received. Using the patented innovations, the "communication device … may respond to packets in an expedited manner (i.e., before the packets have been completely received)." '681 patent at 10:59-62; *see also,* '777 patent at 9:26-29.

29. The Ipsilium patents also teach steps to mitigate issues resulting from any incorrect prediction. For example, once the actual field is received, a comparison of the predicted and received values may be performed. *See* '777 patent at 8:33-39. If those predicted and received values match, the processor can complete the processing, including transmitting a reply packet, and await arrival of the next packet. *See id.* at 8:47-51. If an error is detected, the processor may adjust processing of the packet as necessary, which is likely to still be done before all of the packet data has been received. *See id.* at 8:65-9:17. If necessary it may also cause any reply packets or packet fragments that have already been transmitted to be destroyed or discarded, for example by transmitting a premature end-of-frame delimiter. *See id.* In this way, the invention includes the internal implementation of a custom protocol stack that predicts header fields and processes the

packets based on the predicted header fields before the entire packet is fully received, yet devices operating in accordance with the claimed inventions still conform to and interoperate with conventional network protocols.

CISCO'S INFRINGEMENT OF IPSILIUM'S PATENTS

30. Ipsilium incorporates herein by reference each and every allegation set forth in paragraphs 1 - 29 above.

31. On information and belief, Cisco is the world's largest maker of computer networking equipment. Cisco reported worldwide sales of $42.9 billion and profits of $10.7 billion for its fiscal year 2016. Among the products sold by Cisco are switches, devices that allow network communications between and among computers and other connected devices.

32. There is a significant market for low-latency switches, those with a very short time between when data packets are received at the switch and when reply packets are transmitted from the switch. One group of customers for such products are investment firms known as high frequency traders ("HFTs"). On information and belief, HFTs make a large number of buy and sell transactions in a wide array of securities, attempting to profit from small price discrepancies between market makers. Those price discrepancies are exploited by the first trader to recognize the discrepancy and enter a trading order before its HFT competitors or the rest of the market. As a result, those firms value network speed improvements measured in nanoseconds. Recent published reports estimate that the market for such low-latency switches is over $3 billion per year and growing. On information and belief, Cisco considers this market as critical to its commercial interests. In an interview with eWeek Magazine in 2012, Paul Perez, then Vice President and Chief Technical Officer of Cisco's Data Center Group, stated that the low-latency network switch business represents "billions of dollars of revenue to Cisco" and that "[f]inancial services is a key vertical for [Cisco]."

33. On information and belief, in or about 2004, former Cisco employees incorporated Arista Networks, Inc. to compete with Cisco. In 2008 another key Cisco employee, Jayshree Ullal, joined Arista as its CEO, and Arista launched its first products. Arista introduced 10Gb switches

that provided lower latency at lower cost than Cisco's competing products. *See* Marguerite Reardon, "Sun co-founder Bechtolsheim makes start-up move", CNET, Oct. 23, 2008, *available at* https://www.cnet.com/news/sun-co-founder-bechtolsheim-makes-start-up-move/. Arista's low latency switches were particularly popular among HFTs and other financial services firms, such that by 2009 about 1/3 of Arista's customers were Wall Street trading firms. In 2011 Arista introduced the 7124SX model switch, which at that time claimed the lowest latency of any product available, reportedly 20% faster than previous low-latency switches. *See* Jim Duffy, "Arista Networks drives latency below 500 nanoseconds with data centre switch", Techworld from IDG (Mar. 15, 2011), https://www.techworld.com/news/data/arista-networks-drives-latency-below-500-nanoseconds-with-data-centre-switch-3265074/. On information and belief, in or around 2011 other Cisco competitors, such as Mellanox and Juniper Networks were also introducing low-latency switches that offered better performance than products available from Cisco.

34. On information and belief, Cisco launched a massive development effort – reportedly at a cost of $1 billion – to introduce products to compete in the low-latency switch market. Cisco ultimately created products that not only matched, but exceeded the latency performance of these competitors by choosing to implement the inventions described and claimed in Dr. Hariharasubrahmanian's patents.

35. On or around September 19, 2012, Cisco introduced its Nexus 3548 model switch, with a claimed industry-leading latency. Cisco specifically designed the Nexus 3548 to provide "critical enabling technology" to high speed trading applications where "every nanosecond matters." *See*, *e.g.*, Cisco, "Cisco Algo Boost and Nexus 3548: Breaking 200ns Low Latency Barrier", YouTube (Sept. 20, 2012), https://youtu.be/KT6Fa7MGEX8?t=30s; Cisco, "Cisco Algo Boost: A Game changer in Ultra-Low Latency", YouTube (Sept. 20, 2012), https://youtu.be/fSZ80tHTCcg?t=11s; Berna Devrim, "Introducing Cisco Algo Boost and Nexus 3548 – Breaking 200 ns Latency Barrier!", Cisco Blogs (Sept. 19, 2012), https://blogs.cisco.com/datacenter/cisco-algorithm-boost-and-nexus-3548. At the time, Cisco represented that it had "leapfrogged our competitors in delivering a full featured switch that offers

the lowest latency Ethernet in the networking industry." *See* "Cisco Offers World's Lowest Latency Networking Technology for High Performance Data Center Environments" (Sept. 19, 2012), https://newsroom.cisco.com/press-release-content?articleId=1028561. The Nexus 3548 switches include a Cisco-designed ASIC it calls "Monticello." That chip, along with techniques Cisco calls Algorithm Boost or "Algo Boost" technology, allowed Cisco to achieve what it claimed to be industry-leading latencies.

36. On information and belief, Cisco's design efforts were led by Chih-Tsung Huang, then the Director of Engineering of Cisco's Data Center Group. Mr. Huang and others at Cisco publicly represented that the techniques implemented in the Monticello ASIC of the Nexus 3548 switches to obtain low latency are described in patent applications filed by Cisco. *See*, *e.g.*, Cisco, "Nexus 3548: Inside the Custom ASIC", YouTube (Nov. 13, 2012), https://youtu.be/9IyYl2R1jT0?t=1m23s; Cisco, "Introducing Cisco Algo Boost and Nexus 3548 -- Breaking the 200 ns Latency Barrier!", YouTube (Nov. 13, 2012), https://youtu.be/_p7HPMQdtGc?t=46. At least one such application issued as U.S. Patent 9,065,780 (the "Cisco '780 patent"). On information and belief, Cisco was aware and intended that the '780 Patent specifically disclosed and covered the technology within the Nexus 3548. Mr. Huang, along with others involved in the Monticello chip design, are named as inventors on that patent. Moreover, Cisco filed the release notes for the Cisco Nexus 3000 Series as part of an Information Disclosure Statement ("IDS") for that patent's application with the USPTO on February 14, 2013. And Cisco's Will Ochandarena, Product Manager, explained that the Nexus 3548 is the "newest member of the Nexus 3000 Series Switches." *See* Cisco, "Cisco Nexus 3548 Video Data Sheet", https://video.cisco.com/detail/video/2540582995001/cisco-nexus-3548-video-data-sheet. Further, when describing the Nexus 3548 in promotional videos, Mr. Huang stated that "we actually have patents and techniques" covering the low latency features of the Nexus 3548. *See* Cisco, "Nexus 3548: Inside the Custom ASIC", YouTube (Nov. 13, 2012), https://youtu.be/9IyYl2R1jT0?t=1m23s. Additionally, Cisco's Berna Devrim, then a Senior Manager in Cisco's Data Center Group, stated that Cisco has "numerous patents pending we have

designed, purpose built in fact, … for the high-performance trading environment … groundbreaking network innovations." *See* Cisco, "Introducing Cisco Algo Boost and Nexus 3548 -- Breaking the 200 ns Latency Barrier!", YouTube (Nov. 13, 2012), https://youtu.be/_p7HPMQdtGc?t=46. Thus, on information and belief, the Nexus 3548 switch, and other products including the Monticello ASIC design, operate as described in the Cisco '780 patent.

37. Both the descriptions of the Nexus 3548 given by Mr. Huang as well as the Cisco '780 Patent, for which Mr. Huang is a named inventor, mirror the inventions disclosed in the patents-in-suit. As Mr. Huang explained at the time, in the Nexus 3548 switch, "[e]ven before the packet fully arrived, the headers and everything are already being processed. Right? So that we actually can send out the packet even before the complete packet is received." *See* Cisco, "Nexus 3548: Inside the Custom ASIC", YouTube (Nov. 13, 2012), https://youtu.be/9IyYl2R1jT0?t=7m25s. According to the Cisco '780 patent, the Nexus 3548 achieves low latency by predicting the values of packet header fields before those header fields are received: "One or more header fields not yet available at the network device are predicted based on one or more header fields that are available at the network device." Cisco '780 patent at Abstract. It also states that "[a] network processing decision is generated for the packet based on the predicted one or more header fields and the one or more header fields that are available at the network device." *Id.* at 1:55-60. Finally, it discloses methods for detecting and mitigating any discrepancies between the predicted values and the received values. *Id.* at 4:15-34. These are precisely the innovative techniques described and claimed in the Ipsilium patents. For example, the Ipsilium '777 patent states that "the present inventions . . . permit communications devices to predict one or more fields in packets before the fields are received, thereby . . . permitting the devices to respond to packets before the entire packet is received." '777 patent at 2:12-17.

38. Cisco's misappropriation of Ipsilium's inventions also includes the Nexus 3524 switch, which Cisco represents "is a Cisco Nexus 3548 switch, but with only 24 ports active." *See* "Cisco Nexus 3548 Switch NX-OS Release Notes, Release 6.0(2)A8(3)" (updated Oct. 31, 2016), https://www.cisco.com/c/en/us/td/docs/switches/datacenter/nexus3548/sw/release_notes/602_A8_

3/n3k_relnotes_6_0_2_a_8_3.html. Thus, on information and belief, the Nexus 3524 operates identically to the Nexus 3548 in all aspects relevant to this matter. Both products will be referred to collectively as the "Nexus 3000" switches. Cisco's misappropriation continued at least with the introduction of the UCS Mini 6324 product in 2014. On information and belief, the UCS Mini 6324 contains the same Monticello ASIC, which Cisco renamed Malibu for that product. On information and belief, the operation of the UCS Mini 6324 is in all relevant aspects the same or equivalent to that of the Nexus 3000 switches. A Cisco employee has stated that the Malibu ASIC is the same as the Monticello, "only with less [sic] ports" and achieves the same latency performance. *See* "Ask the Expert: Cisco Nexus 3000 Series Switches" (Sept. 21, 2015), https://supportforums.cisco.com/discussion/12611691/ask-expert-cisco-nexus-3000-series-switches.

39. Upon information and belief, Cisco intends to incorporate the Nexus 3548 chip technology into additional products, as Cisco's Rajan Panchanathan, then Director of Product Management, stated that "while the Nexus 3548 will be the first to offer Algo Boost, the chip technology will find its way into future generations of all Nexus switches." Jeff Burt, "Cisco, Arista Unveil Low-Latency Ethernet Networking Switches", eWeek.com (Sept. 19, 2012), http://www.eweek.com/networking/cisco-arista-unveil-low-latency-ethernet-networking-switches. Thus, the Nexus 3000 switches, the UCS Mini 6324, any other Cisco products implementing the Algo Boost technology, any other Cisco products that have a substantially similar ASIC, and/or any other Cisco products that perform header prediction and packet processing in substantially the same manner, are collectively referred to as "the Accused Products."

CISCO'S INFRINGEMENT OF IPSILIUM'S PATENTS IS WILLFUL

40. Ipsilium incorporates herein by reference each and every allegation set forth in paragraphs 1 - 39 above.

41. Ipsilium's inventions were disclosed in patent applications published nearly ten years before Cisco introduced its infringing products. The '681 patent issued in November 2004 and the '777 in November 2005. Cisco was repeatedly made aware of these patented inventions both before

and shortly after it began its infringing activities by multiple patent offices on multiple occasions. For example, on May 4, 2005 the '681 patent was cited by the USPTO examiner during prosecution of Cisco's patent application no. 10/044,665 entitled "Method of Point-to-Point Protocol Negotiation." Thus, Cisco was aware of the Ipsilium patents well before it developed the Accused Products.

42. On February 14, 2013 Cisco filed a utility patent application which lead to the issuance of the '780 patent, claiming priority to an earlier provisional application filed on September 18, 2012. Cisco also filed an application with the European Patent Office ("EPO") pursuant to the Patent Cooperation Treaty seeking patent coverage similar to that in the '780 application. On or about December 11, 2013 the EPO sent Cisco the result of its prior art search informing Cisco that it was not entitled to the patent claims it sought because of the PCT counterpart to the Ipsilium patents. On December 27, 2013 Cisco filed an IDS with the USPTO disclosing this PCT reference, confirming Cisco's knowledge of Dr. Hariharasubrahmanian's invention and its relevance to the Accused Products.

43. Despite knowing of the '681 patent since May 4, 2005, in its application for the '780 patent, Cisco claimed to have invented exactly what is covered by Ipsilium's issued patent. For example, the original claim 1 of the Cisco '780 patent application read:

> 1. A method comprising:
>
> at a network device, receiving a packet that includes a plurality of header fields;
>
> parsing the packet to sequentially obtain the plurality of header fields;
>
> predicting one or more header fields not yet available at the network device based on one or more header fields that are available at the network device; and
>
> generating a network processing decision for the packet based on the predicted one or more header fields and the one or more header fields that are available at the network device.

44. Comparing that claim as Cisco originally applied for to claim 1 of Ipsilium's '681 patent readily shows that Cisco's engineers—including '780 inventor and then Director of Engineering for the Nexus 3548, Mr. Huang—adopted precisely the inventive solution disclosed by

Dr. Hariharasubrahmanian nearly fourteen years earlier. Claim 1 of the '681 patent is as follows, with like colors indicating the essentially identical elements of both claims:

> **1**. A method for predicting one or more fields of a packet having a plurality of fields, the packet belonging to a set of packets, each of the fields containing data representing a value, the method comprising:
>
> receiving one or more of the fields of the packet;
>
> analyzing a first value of at least one of the received fields;
>
> predicting a second value of at least one other field of the packet not yet received, based on a correlation between the first value and a property of the at least one other field not yet received; and
>
> processing the packet based on the one or more received fields and the predicted at least one other field.

45. Unsurprisingly, the USPTO rejected Cisco's proposed claims in light of the patents-in-suit on October 23, 2014. Cisco filed no argument to explain how its invention differed from Dr. Hariharasubrahmanian's. Instead Cisco conceded that it was not entitled to the originally-filed claims that were identical to Ipsilium's patents by amending and narrowing its claims on January 1, 2015.

46. As Cisco was aware of Ipsilium's patents well before it began development of the Nexus 3548, through the development and release of all the Accused Products, Cisco knew, should have known, or was willfully blind to the fact that all the Accused Products infringe Ipsilium's patents. Further, as described above, on information and belief, the Cisco '780 Patent was filed to cover the Accused Products. Thus, when Cisco was again reminded by both the EPO and the USPTO during prosecution of Cisco's '780 Patent, Cisco knew that all the Accused Products infringed Ipsilium's patents and Cisco should have removed the infringing devices or sought to obtain a license to the patents. Cisco's infringement is therefore deliberate and willful.

COUNT I

(Willful Infringement of the '681 Patent)

47. Ipsilium incorporates herein by reference each and every allegation set forth in paragraphs 1 - 46 above.

48. The '681 patent was duly and lawfully issued by the U.S. Patent and Trademark Office and represents a significant advance in computer networking technology over previously known instruments and techniques.

49. The '681 patent concludes with 57 claims directed to the inventive methods, systems, computer-readable instructions and devices described, including 12 independent claims.

50. Cisco directly infringes the '681 patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, selling, offering to sell and/or importing into this country systems that embody the patented invention, including the Accused Products based on the Monticello ASIC design. For example, upon information and belief, Cisco has at least sold the accused Nexus 3548 and 3524 to NASDAQ, Advantage Futures, Knight Capital Group, BNY Mellon, Credit Suisse, and Morgan Stanley in the United States. Further, upon information and belief, Cisco has sold the accused UCS 6324 to at least "2,200 customers." *See* Satinder Sethi, "Cisco UCS – Driving the Evolution of IT" (Apr. 12, 2016), http://www.cisco.com/c/dam/m/en_emear/events/2016/emeardcpc2016/pdfs/day_1/Cisco_UCS_Driving_the_Evolution_of_IT-Sethi.pdf. On information and belief many of those customers are located within the United States.

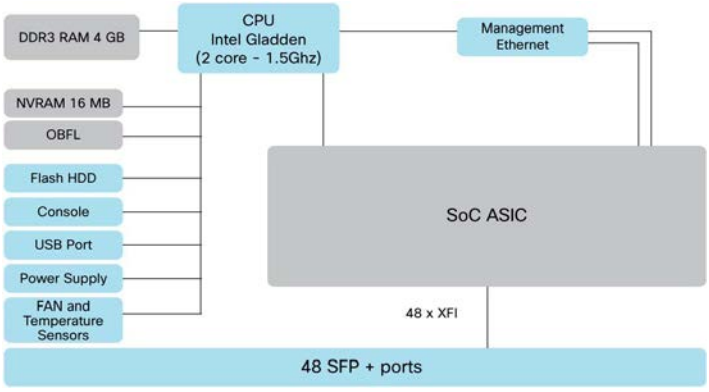
51. For purposes of example only and without limitation, the Accused Products include every limitation of at least independent claim 18 of the '681 patent. Claim 18 of the '681 patent recites:

> 18. A system for predicting one or more fields of a packet having a plurality of fields containing data, such a packet belonging to a set of packets, the system comprising:
>
> [a] a memory configured to store instructions; and
>
> [b] a processor configured to execute the instructions to receive one or more fields of the packet, to determine a first value of at least one of the received fields, to

predict a second value of one or more other fields not yet received based on a correlation between the first value and a property of one or more other fields not yet received and to process the packet based on the one or more received fields and the predicted one or more other fields wherein the processor, when processing the packet, is configured to generate a reply packet based on the at least one received field and the predicted one or more other fields.

52. On information and belief, the accused Cisco products comprise systems for predicting one or more fields of a packet having a plurality of fields containing data, with such a packet belonging to a set of packets.

53. On information and belief, the accused Cisco products include memories configured to store instructions. Such memories include at least the DDR3 RAM and NVRAM available to the CPU as shown in Cisco's schematic diagram of the Nexus 3548 copied below.



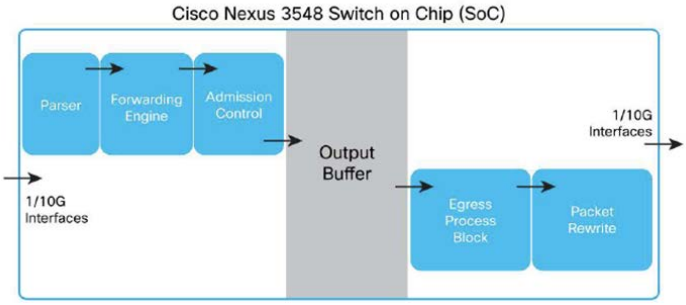
On information and belief, the Monticello SoC ASIC also includes memory configured to store the instructions used to control packet processing, including instructions for predicting packet data values before those values have been received.

54. On information and belief, the Accused Products include a processor configured to execute the instructions to receive one or more fields of the packet, to determine a first value of at least one of the received fields, to predict a second value of one or more other fields not yet received based on a correlation between the first value and a property of one or more other fields not yet received and to process the packet based on the one or more received fields and the predicted one

or more other fields wherein the processor, when processing the packet, is configured to generate a reply packet based on the at least one received field and the predicted one or more other fields.

55. On information and belief, the Accused Products include a processor configured to receive one or more fields of the packet. As shown in the figure below describing the operation of the Nexus 3548 switch, packets are received at the "1/10G Interfaces" and passed to the "Parser" as part of the packet flow.

Figure 3. Cisco Nexus 3500 Switch-on-Chip Packet Flow



Further, as described in Cisco's patent describing Cisco's Nexus 3548, the device "receives a packet that includes a plurality of header fields." Cisco '780 Patent at Abstract.

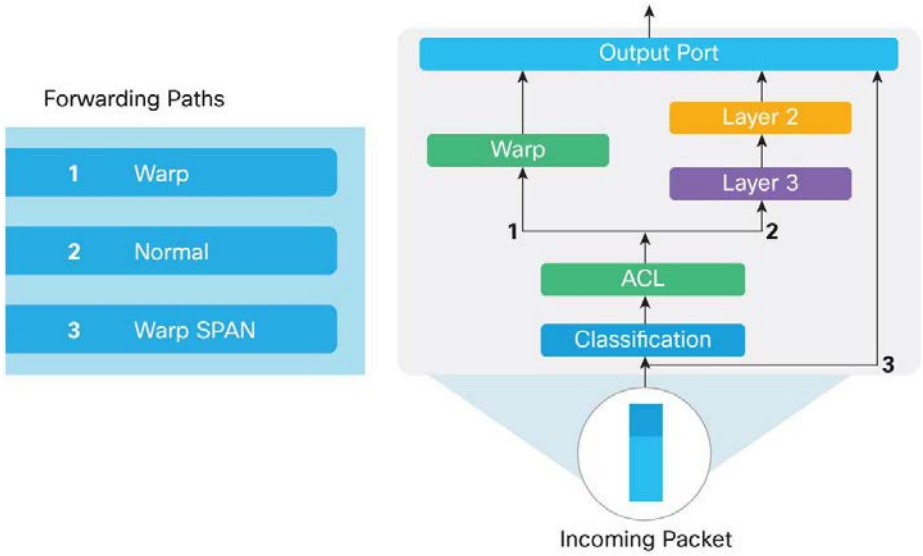
56. On information and belief, the Accused Products include a processor configured to determine a first value of at least one of the received fields. That logic includes but is not limited to functionality described by Cisco as a "parser" or "parser engine." "The parser engine parses the incoming packets and extracts the fields required for decisions and passes the information to the Layer 2 and 3 lookup processes." "Nexus 3548 Switch Architecture" (Sept. 2012), at 6 ("White Paper"). Further, as described in Cisco's '780 patent, "[t]he parser 50 comprises digital logic configured to parse fields of a received packet as the bits of the packet are received at a port of the network device." Cisco '780 Patent at 2:49-51.

57. The Accused Products include a processor configured to predict a second value of the one or more fields based on a correlation between the first value and a property of the one or more other fields not yet received: "The L3 header prediction unit 100 is configured to predict the L3 headers based on the L2 headers, before the L3 headers 82 have been parsed and are available for processing at the network device. Thus, the L3 header prediction unit 100 will output a prediction

of the L3 headers (predicted second set of header fields) for a packet based on the received L2 headers (received first set of header fields) of that packet." Cisco '780 Patent at 3:63-4:2. The Cisco '780 Patent discloses that various correlations based on the received fields and not yet received header fields are used to make these predictions. For example the Cisco Patent explains: "Packet flows are bursty packets which are likely to arrive in identical trains, often reproducing the same flow many times. It is useful to record the previous packet's headers to be used as a key to lookup and predict the headers for the current packet. For example, when packets arrive their headers are stored as a key to a flow history cache in which the result data is the next packet's headers. In the future, when the same packet arrives, its headers are used to lookup the prediction for the next packet's headers." Cisco '780 Patent at 5:48-56. And: "Header prediction logic used by the L3 header prediction unit 100 can be implemented in several ways. With reference now to FIG. 4A, one example method for L3 header prediction is to cache the headers of recent packets. FIG. 4A shows an example cache 120 containing a table of L2 headers and L3 headers of packets received by the network device over time. In this example, the 'key' to the cache is the L2 headers and the stored/cached value is its L3 headers. When a new packet arrives, its L2 headers information is looked up in the cache to obtain a prediction for the L3 headers in significantly less time than it takes for the L3 headers to be fully parsed and made available for processing." Cisco '780 Patent at 4:54-65.

58. On information and belief, the Accused Products include a processor configured to process the packet based on the one or more received fields and the predicted one or more other fields, for example: "The L3 predictive network processing unit 112 is configured to generate a predicted L3 network processing decision based on the L2 result and the predicted L3 headers." Cisco '780 Patent at 4:3-5, Figure 3.

59. On information and belief, the Accused Products include a processor configured to generate a reply packet based on the at least one received field and the predicted one or more other fields: "[t]he predictive processing SIB 40 makes decisions including, but not limited to security, quality of service (QoS), statistics, ingress and egress access control policies, classification, marking, adding or deletion of packet fields, load balancing, multi-tenancy handling, Layer 2 bridging (switching), Layer 3 routing, and dropping of packets." Cisco '780 Patent at 2:17-24. Further, the reply packets is sent out of the appropriate output port, as shown in Fig. 4 from the Nexus 3548 Switch Architecture White Paper:



60. On information and belief, the instructions controlling the operations performed by the processor in the Accused Product as described above are stored in a computer-readable form in one or more memory devices in those products. For the forgoing reasons, the Accused Products include computer-readable media that store instructions executable by the processor that encompass every limitation of one or more of claims 30 – 43 and 54 of the '681 patent.

61. On information and belief, when operating as described above, the Accused Products perform methods of predicting packet values and processing packets that infringe one or more of claims 1-15 and 56 of the '681 patent. On information and belief, Cisco has used and continues to use the Accused Products in the United States to perform the claimed methods and therefore has

directly infringed and continues to directly infringe those claims, literally or under the doctrine of equivalents, pursuant to 35 U.S.C. §271(a). Furthermore, Cisco's customers use the Accused Products in an infringing manner as shown by, for example, Advantage Futures stating that "[c]urrently, the fastest edge switch available is the Cisco NX 3548. [] We implemented them on the CME edge so that our clients could benefit . . . ." "The Race to Zero", Inside Advantage (2014), at 7, http://www.advantagefutures.com/wp-content/uploads/Inside_Advantage_Fall_2014.pdf. Cisco supplies the Accused Products to its end customers in the United States along with all necessary firmware, software and support to enable those customers to use the Accused Products for their intended purpose. Cisco has been and continues to be aware of that infringement and, by supplying the Accused Products, intends for its customers to infringe the '681 patent. Cisco is therefore liable for inducing its customers' infringement pursuant to 35 U.S.C. §271(b).

62. As explained above in ¶¶ 40-46, the willfulness section, Cisco has been aware of the '681 patent since at least 2005 and has known, should have known, or was willfully blind to the fact that all the Accused Products infringe the '681 patent. On information and belief Cisco has no good faith basis on which to conclude that it does not infringe one or more valid and enforceable claims of the '681 patent. Despite that knowledge, Cisco has continued to infringe and has not made any effort to curtail that infringement and has no intention of curtailing that infringement unless ordered to do so. Cisco's infringement is therefore egregious, wanton and malicious.

COUNT II

(Willful Infringement of the '777 Patent)

63. Ipsilium incorporates herein by reference each and every allegation set forth in paragraphs 1 - 62 above.

64. The '777 patent was duly and lawfully issued by the U.S. Patent and Trademark Office and represents a significant advance in computer networking technology over previously known instruments and techniques.

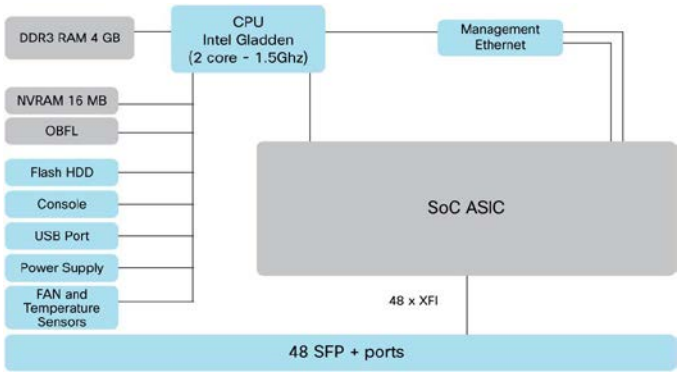
65. The '777 patent concludes with 57 claims directed to the inventive methods, systems, computer-readable instructions and devices described, including 12 independent claims.

66. Cisco has directly infringed and continues to directly infringe the '777 patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, selling, offering to sell and/or importing into this country systems that embody the patented invention, including the Accused Products based on the Monticello ASIC design. For example, upon information and belief, Cisco has at least sold the accused Nexus 3548 and 3524 to NASDAQ, Advantage Futures, Knight Capital Group, BNY Mellon, Credit Suisse, and Morgan Stanley. Further, upon information and belief, Cisco has sold the accused UCS 6324 to at least "2,200 customers." *See* "Cisco UCS – Driving the Evolution of IT", *available at*, http://www.cisco.com/c/dam/m/en_emear/events/2016/emeardcpc2016/pdfs/day_1/Cisco_UCS_Driving_the_Evolution_of_IT-Sethi.pdf. On information and belief many of those customers are located within the United States.

67. For purposes of example only and without limitation, the Accused Products include every limitation of Claims 17 and 18 of the '777 patent. Claim 17 reads as follows:

> 17. A system for predicting one or more fields of a packet having a plurality of fields, each of the fields storing data representing a value, the system comprising:
>
> a memory configured to store instructions; and
>
> a processor configured to execute the instructions to [i] receive one or more fields of the packet, [ii] determine the value of at least one of the received fields, [iii] predict how the packet will be processed by upper level protocols, application protocols or both based on the value of the obtained field and further predict a value of one or more other fields not yet received based on the value of the at least one received field, and [iv] process the packet based on the one or more received fields and the predicted one or more other fields.

68. On information and belief, the accused Cisco products include memories configured to store instructions. Such memories include at least the DDR3 RAM and NVRAM available to the CPU as shown in Cisco's schematic diagram of the Nexus 3548 copied below.

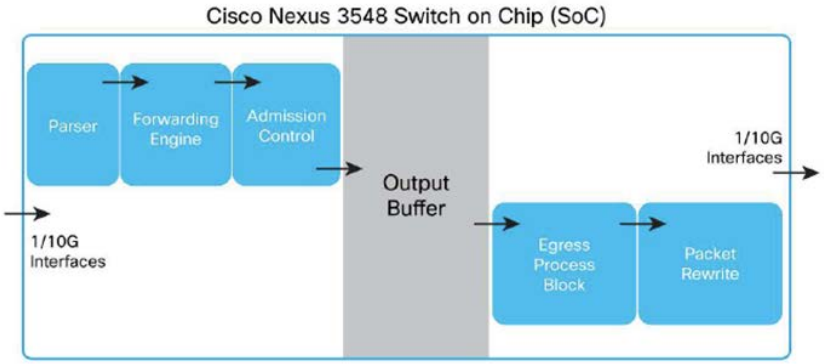


On information and belief, the Monticello SoC ASIC also includes memory configured to store the instructions used to control packet processing, including instructions for predicting packet data values before those values have been received.

69. On information and belief, the Accused Products include a processor configured to execute the instructions to receive one or more fields of the packet, determine the value of at least one of the received fields, predict how the packet will be processed by upper level protocols, application protocols or both based on the value of the obtained field and further predict a value of one or more other fields not yet received based on the value of the at least one received field, and process the packet based on the one or more received fields and the predicted one or more other fields.

70. On information and belief, the Accused Products include a processor configured execute instructions to receive one or more fields of the packet. As shown in the figure below describing the operation of the Nexus 3548 switch, packets are received at the "1/10G Interfaces" and passed to the "Parser" as part of the packet flow. Further, as described in Cisco's patent describing Cisco's Nexus 3548, the device "receives a packet that includes a plurality of header fields." Cisco '780 Patent at Abstract.

Figure 3. Cisco Nexus 3500 Switch-on-Chip Packet Flow

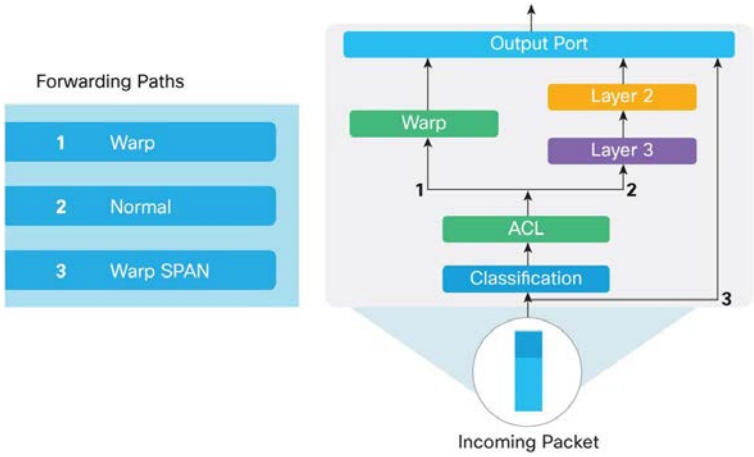


71. On information and belief, the Accused Products include a processor configured to determine the value of at least one of the received fields. That processor includes but is not limited to functionality described by Cisco as a "parser" or "parser engine." "The parser engine parses the incoming packets and extracts the fields required for decisions and passes the information to the Layer 2 and 3 lookup processes." Nexus 3548 Switch Architecture White Paper at 6. Further, as described in Cisco's patent describing the Nexus 3548, "[t]he parser 50 comprises digital logic configured to parse fields of a received packet as the bits of the packet are received at a port of the network device." Cisco '780 Patent at 2: 49-51.

72. On information and belief, the Accused Products include a processor executing instructions to predict how the packet will be processed by upper level protocols, application protocols or both based on the value of the obtained field and further predict a value of one or more other fields not yet received based on the value of the at least one received field, and process the packet based on the one or more received fields and the predicted one or more other fields. As one example, a received lower-level L2 header field is used to predict the value of a not yet received header field that belongs to the upper-level L3 protocol: "The L2 result is supplied as input to the L3 predictive network processing unit 112 and to the L3 network processing unit 114." Cisco '780 Patent at 3:51-62. "The L3 header prediction unit 100 is configured to predict the L3 headers based on the L2 headers, before the L3 headers 82 have been parsed and are available for processing at the network device. Thus, the L3 header prediction unit 100 will output a prediction of the L3 headers (predicted second set of header fields) for a packet based on the received L2 headers

(received first set of header fields) of that packet." Cisco '780 Patent at 3:63-4:2. Further, "[t]he L3 predictive network processing unit 112 is configured to generate a predicted L3 network processing decision based on the L2 result and the predicted L3 headers." *Id.* at 4:3-5.

73. The Accused Products also meet every limitation of dependent claim 18 of the '777 patent. Claim 18 reads: "The system of claim 17, wherein when processing the packet, the processor is configured to generate a reply packet based on the one or more received fields and the predicted one or more other fields." On information and belief, the Accused Products include a processor configured to generate a reply packet based on the at least one received field and the predicted one or more other fields: "[t]he predictive processing SIB 40 makes decisions including, but not limited to security, quality of service (QoS), statistics, ingress and egress access control policies, classification, marking, adding or deletion of packet fields, load balancing, multi-tenancy handling, Layer 2 bridging (switching), Layer 3 routing, and dropping of packets." Cisco '780 Patent at 2:17-24. Further, the reply packets is sent out of the appropriate output port as shown in Fig. 4 from the Nexus 3548 Switch Architecture White Paper:



74. On information and belief, the instructions controlling the operations performed by the processor in the Accused Product as described above are stored in a computer-readable form in one or more memory devices in those products. For the forgoing reasons, the Accused Products include computer-readable media that store instructions executable by the processor that encompass every limitation of one or more of claims 30 – 43 of the '777 patent and Cisco directly infringes

those claims pursuant to 35 U.S.C. §271(a) by making, using, selling, offering to sell and/or importing the Accused Products.

75. On information and belief, for the reasons set forth above, when operating as intended the Accused Products perform methods of predicting packet values and processing packets that meet every limitation of one or more of claims 1-15 and 56 of the '777 patent. On information and belief, Cisco has used and continues to use the Accused Products in the United States to perform the claimed methods and therefore has directly infringed and continues to directly infringe those claims, literally or under the doctrine of equivalents, pursuant to 35 U.S.C. §271(a). Furthermore, Cisco's customers use the Accused Products in an infringing manner as shown by, for example, Advantage Futures stating that "[c]urrently, the fastest edge switch available is the Cisco NX 3548. [] We implemented them on the CME edge so that our clients could benefit . . . ." "The Race to Zero", Inside Advantage (2014), at 7, http://www.advantagefutures.com/wp-content/uploads/Inside_Advantage_Fall_2014.pdf. Cisco supplies the Accused Products to its end customers in the United States along with all necessary firmware, software, instructions and support to enable and encourage those customers to use the Accused Products to perform the claimed methods. Cisco has been and continues to be aware of that its customers are infringing infringement and by supplying the Accused Products Cisco intends for its customers to infringe the '777 patent. Cisco is therefore liable for inducing its customers' infringement pursuant to 35 U.S.C. §271(b).

76. As stated above in ¶¶ 40-46, Cisco has been aware of the related '681 patent since at least 2005, the related Ipsilium WO application since at least 2013, and the '777 patent since at least December 2013. Cisco has known, should have known, or was willfully blind to the fact that all the Accused Products infringe the '777 patent. On information and belief Cisco has no good faith basis on which to conclude that the Accused Products do not infringe one or more valid and enforceable claims of the '777 patent. Despite that knowledge, Cisco has intentionally continued to infringe and has not made any effort to curtail that infringement and has no intention of curtailing that infringement unless ordered to do so. Cisco's infringement is therefore egregious, wanton and malicious.

PRAYER FOR RELIEF

WHEREFORE, Ipsilium prays for relief as follows:

A. Judgment that Cisco has infringed and continues to infringe one or more claims of the '681 patent;

B. Judgment that Cisco has infringed and continues to infringe one or more claims of the '777 patent;

C. Judgment that Cisco's infringement is and has been willful;

D. Judgment that this is an exceptional case pursuant to 35 U.S.C. § 285;

E. An Order enjoining Cisco and all those acting in concert with it from any future acts of infringement of the patents-in-suit;

F. An Order that Cisco pay plaintiff damages in an amount adequate to compensate for the infringement of no less than a reasonable royalty, increased three times, along with pre-judgment and post-judgment interest;

G. An Order that Cisco pay Ipsilium's reasonable costs and attorneys' fees incurred in this matter; and

H. Such other and further relief as the Court deems just and warranted.

Respectfully submitted,

DATED: December 18, 2017

By /s/ Sean P. DeBruine
Sean P. DeBruine

Attorney for Plaintiff
IPSILIUM LLC

DEMAND FOR JURY TRIAL

Ipsilium demands a jury trial on all issues so triable.

Respectfully submitted,

DATED: December 18, 2017

By /s/ Sean P. DeBruine
Sean P. DeBruine

Attorney for Plaintiff
IPSILIUM LLC